**REMARKS**

Applicants appreciate the Examiner's thorough examination of the present application as evidenced by the final Office Action of October 11, 2002 and the Advisory Action of December 30, 2002. Applicants especially appreciate the indication that Claims 28 and 29 have been allowed and that Claims 5, 10, and 18 recite patentable subject matter. To advance prosecution and to facilitate an early allowance of the present application, Applicants have amended independent Claim 1 to incorporate recitations from allowable dependent Claim 5, which has been canceled without prejudice or disclaimer. In addition, Applicants have amended independent Claims 12 and 20 to incorporate recitations similar to dependent Claim 5. Dependent Claims 3, 14, and 22 have been amended to maintain consistency with independent Claims 1, 12, and 20. Applicants respectfully submit that independent Claims 12 and 20 are allowable for at least the reasons that dependent Claim 5 is allowable. Independent Claims 12 and 20, however, also stand rejected under 35 U.S.C. §112, ¶2 as being indefinite. In response, Applicants have amended independent Claims 20 and 30 along with dependent Claims 21, 22, and 24 - 26 to numerically note the various references to "logic." Applicants respectfully submit that Claims 20 - 22, 24 - 27, and 30 satisfy the requirements of 35 U.S.C. §112.

In light of the above amendments and remarks, Applicants respectfully submit that the above-entitled application is now in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

It is not believed that an extension of time and/or additional fee(s), including fees for net addition of claims, are required, beyond those that may otherwise be provided for in documents accompanying this paper. In the event, however, that an extension of time is necessary to allow consideration of this paper, such an extension is hereby petitioned under 37 C.F.R. §1.136(a). Any additional fees believed to be due in connection with this paper may be charged to IBM's Deposit Account No. 09-1990.

Respectfully submitted,

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**Customer Number:**

20792
PATENT TRADEMARK OFFICE

**CERTIFICATE OF FACSIMILE TRANSMISSION**

I hereby certify that this Response After Final dated February 10, 2003 is being transmitted via facsimile to P. Kumar, Group 2631, United States Patent and Trademark Office at 703-872-9315 on the date shown below.

Traci A. Brown
Date of Signature: February 10, 2003

## VERSION WITH MARKINGS TO SHOW CHANGES MADE

**In the Claims:**

Please amend the following Claims by adding the language that is underlined ("__") and by deleting the language that is enclosed within brackets ("[ ]"):

1. (Twice Amended) A receiver for demodulating a data signal transmitted from a digital source at a network sampling rate that is synchronized with a network clock, comprising:

a two-stage interpolator, responsive to digital samples of the data signal, that generates interpolated digital samples in response thereto, the digital samples having a first local sample rate that is synchronized with a local clock and the interpolated digital samples having a second local sample rate that is synchronized with the network clock, the two-stage interpolator comprising:

a time converter, responsive to a sampling index signal, that generates first and second integers in response thereto;

a polyphase interpolator, responsive to the digital samples of the data signal and the first integer, that generates first and second estimates for each of the digital samples of the data signal; and

a linear interpolator, responsive to the first and second estimates and the second integer, that generates the interpolated digital samples;

an adaptive fractionally spaced decision feedback equalizer, responsive to the interpolated digital samples, that generates equalized digital samples at the network sampling rate in synchronization with the network clock; and

a slicer, responsive to the equalized digital samples, that generates detected symbols therefrom corresponding to data from the data signal.

3. (Amended) A receiver as recited in Claim 1, further comprising a clock synchronizer responsive to the detected symbols and generating [a] the sampling index signal[, the two stage interpolator being responsive to the sampling index signal].

Please cancel Claim 5 without prejudice or disclaimer.

12. (Twice Amended) A method for demodulating, in a receiver, a data signal transmitted from a digital source at a network sampling rate that is synchronized with a network clock, comprising the steps of:

sampling the data signal to produce digital samples at a first local sample rate that is synchronized with a local clock;

generating first and second integers in response to a sampling index signal using a time converter;

interpolating the digital samples in response to the first integer to produce first and second estimates for each of the digital samples using a polyphase interpolator;

interpolating the first and second estimates in response to the second integer to produce interpolated digital samples having a second local sample rate that is synchronized with the network clock using a linear interpolator;

equalizing the interpolated digital samples to produce equalized digital samples; and

decoding the equalized digital samples to generate detected symbols therefrom.

14. (Amended) A method as recited in Claim 12, further comprising the step of:

maintaining the synchronization between the second local sample rate and the network clock via [a] the sampling index signal.

20. (Twice Amended) A computer program product for demodulating, in a receiver, a data signal transmitted from a digital source at a network sampling rate that is synchronized with a network clock, comprising:

a computer readable storage medium having computer readable code means embodied therein, the computer readable code means comprising:

first logic configured to sample the data signal to produce digital samples at a first local sample rate that is synchronized with a local clock;

second logic configured to generate first and second integers in response to a sampling index signal using a time converter;

[first] third logic configured to interpolate the digital samples in response to the first integer to produce first and second estimates for each of the digital samples, the [first] third logic configured to interpolate comprising:

fourth logic configured to use a polyphase interpolator to produce the first and second estimates;

[second] fifth logic configured to interpolate the first and second estimates in response to the second integer to produce interpolated digital samples having a second local sample rate that is synchronized with the network clock, the second logic configured to interpolate comprising:

sixth logic configured to use a linear interpolator to produce the interpolated digital samples;

seventh logic configured to equalize the interpolated digital samples to produce equalized digital samples; and

eighth logic configured to decode the equalized digital samples to generate detected symbols therefrom.

21. (Amended) A computer program product as recited in Claim 20, wherein the seventh logic configured to equalize comprises:

ninth logic configured to use an adaptively fractionally spaced decision feedback equalizer that has tap spacing given by $pT/q$ where $T$ is a modulation interval associated with the network sampling rate and $p$ and $q$ are integers to produce the equalized digital samples.

22. (Amended) A computer program product as recited in Claim 20, further comprising:

ninth logic configured to maintain the synchronization between the second local sampling rate and the network clock via [a] the sampling index signal.

24. (Amended) A computer program product as recited in Claim 20, wherein the

receiver further includes an echo canceller coupling a transmitter to the receiver, further comprising:

ninth logic configured to receive at an input of the echo canceller transmit symbols from the transmitter that have a third local sample rate that is synchronized with the local clock; and

tenth logic configured to generate at an output of the echo canceller echo cancellation samples at the first local sample rate in synchronization with the local clock.

25. (Amended) A computer program product as recited in Claim 20, further comprising[;]:

ninth logic configured to identify a signaling alphabet, the eighth logic configured to decode being responsive to the logic configured to identify.

26. (Amended) A computer program product as recited in Claim 25, wherein the ninth logic configured to identify comprises:

tenth logic configured to establish a plurality of alphabet thresholds corresponding to valid data symbols;

eleventh logic configured to compute an average value for the equalized digital samples corresponding to a particular alphabet threshold; and

twelfth logic configured to update the particular alphabet threshold with the average value.

30. (Amended) A computer program product for demodulating, in a receiver, a data signal transmitted from a digital source at a network sampling rate that is synchronized with a network clock, comprising:

a computer readable storage medium having computer readable code means embodied therein, the computer readable code means comprising:

first logic configured to sample the data signal to produce digital samples at a first local sample rate that is synchronized with a local clock;

[first] second logic configured to interpolate the digital samples to produce first and second estimates for each of the digital samples;

[second] third logic configured to interpolate the first and second estimates to produce interpolated digital samples having a second local sample rate that is synchronized with the network clock;

fourth logic configured to equalize the interpolated digital samples to produce equalized digital samples;

fifth logic configured to decode the equalized digital samples to generate detected symbols therefrom;

sixth logic configured to identify a signaling alphabet, the fifth logic configured to decode being responsive to the logic configured to identify, the sixth logic configured to identify comprising:

seventh logic configured to establish a plurality of alphabet thresholds corresponding to valid data symbols;

eighth logic configured to compute an average value for the equalized digital samples corresponding to a particular alphabet threshold; and

ninth logic configured to update the particular alphabet threshold with the average value.